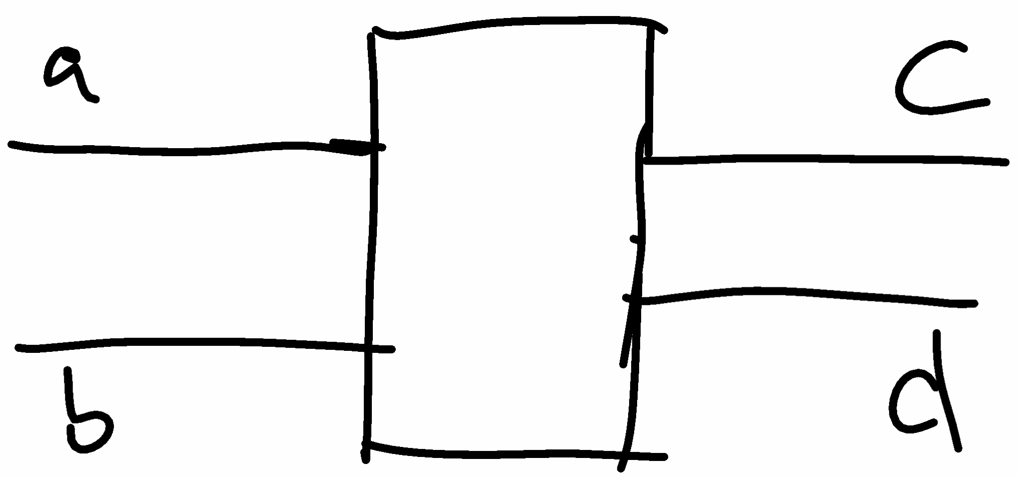
LOGIC GATES & CIRCUITS

Wed 10 Oct 2018

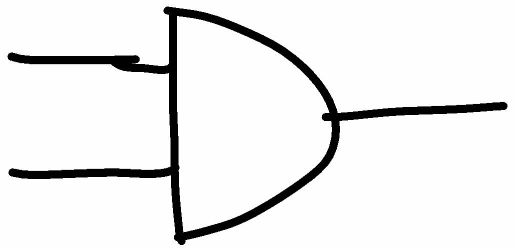
CLASSICAL GATES



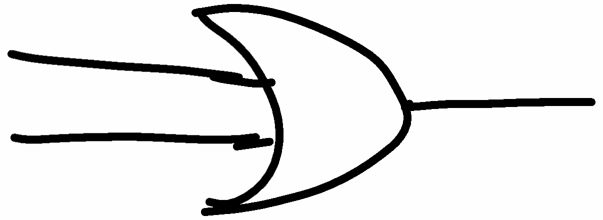
Drawing of a circuit w/ 2 input 2 output

a	b	c
0	0	0
0	1	0
1	0	0
1	1	1

≡ AND

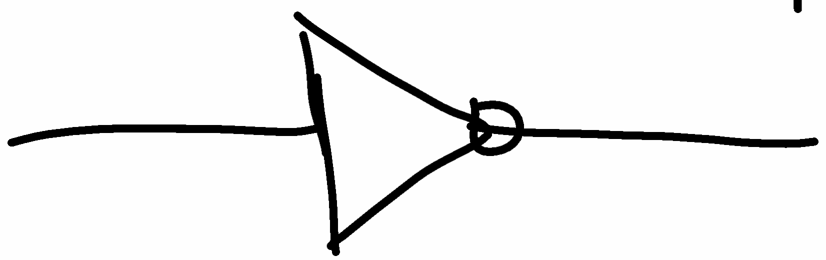


OR



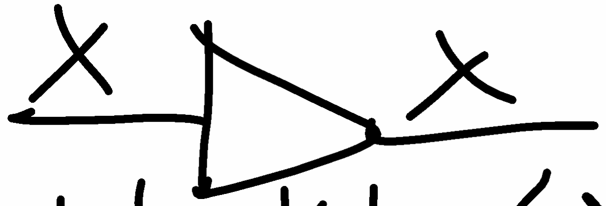
a	b	c
0	0	0
0	1	1
1	0	1
1	1	1

NOT



a	c
0	1
1	0

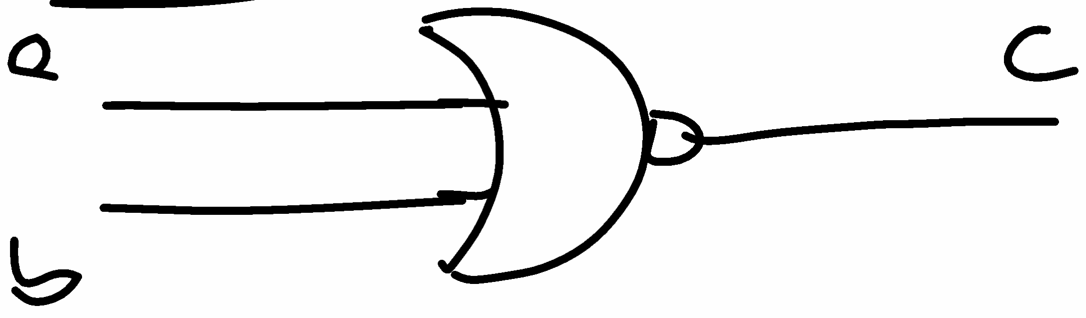
MOST BASIC:



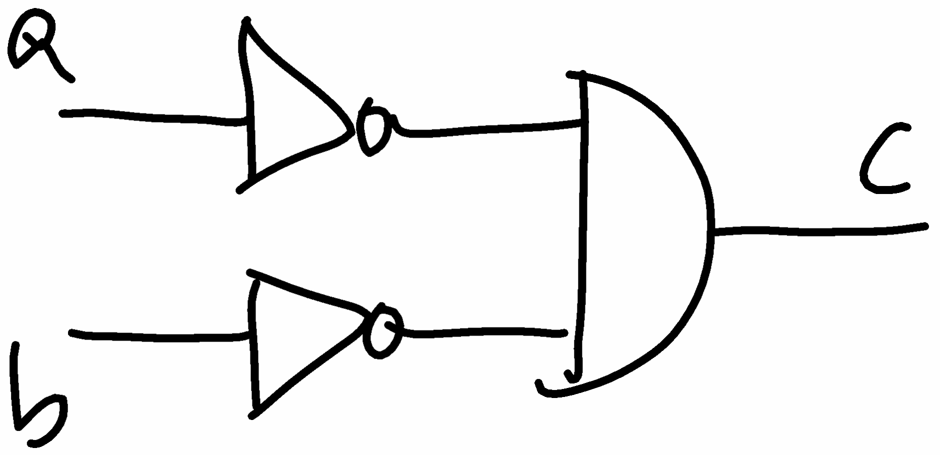
Identity Gate

AND, OR, NOT is a COMPLETE SET OF GATES: MEANS ANY OTHER CAN BE WRITTEN w/ THESE ONLY

NOR



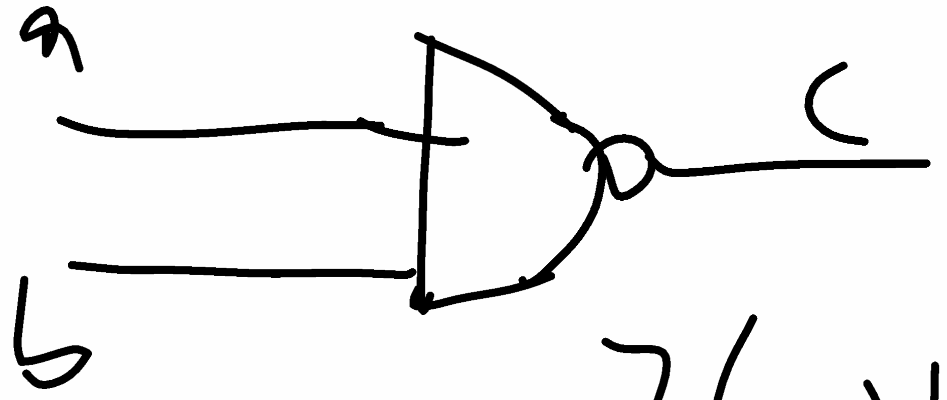
$\equiv$



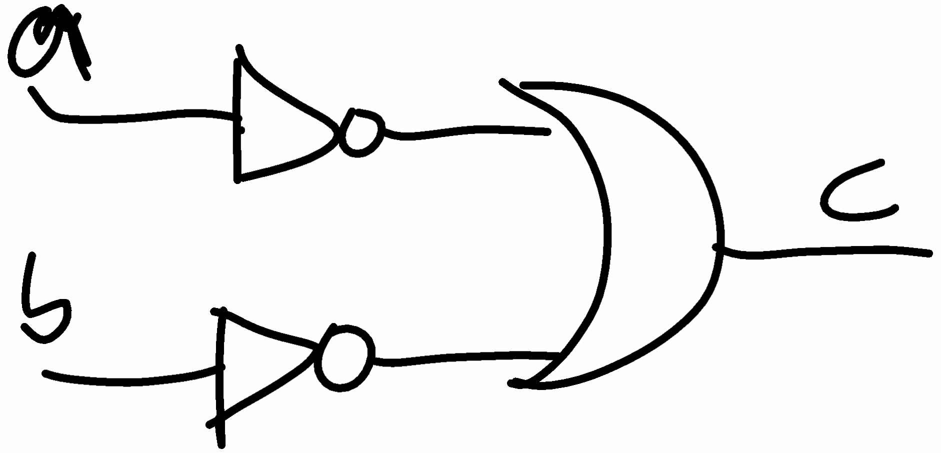
$$c = \neg(a \vee b)$$

$$\equiv \neg a \wedge \neg b$$

NAND

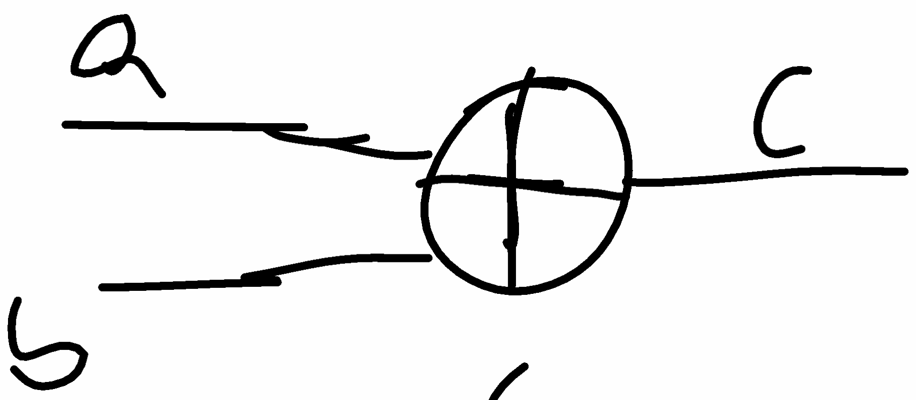


$\equiv$

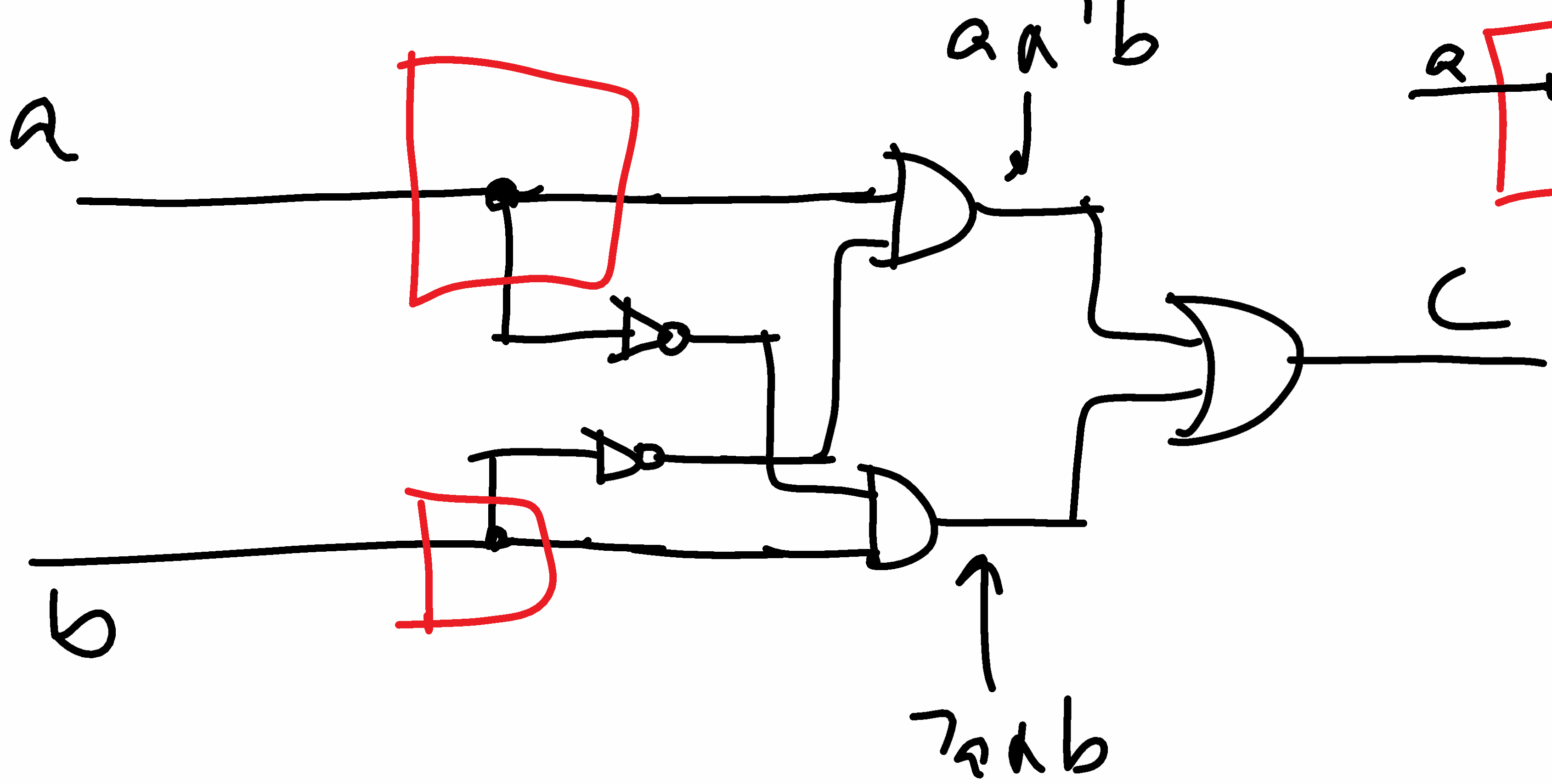


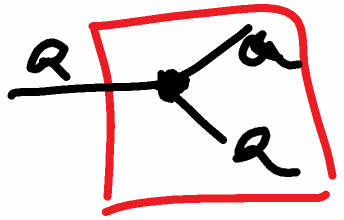
$$c = \neg(a \wedge b) = \neg a \vee \neg b$$

XOR



$\equiv$





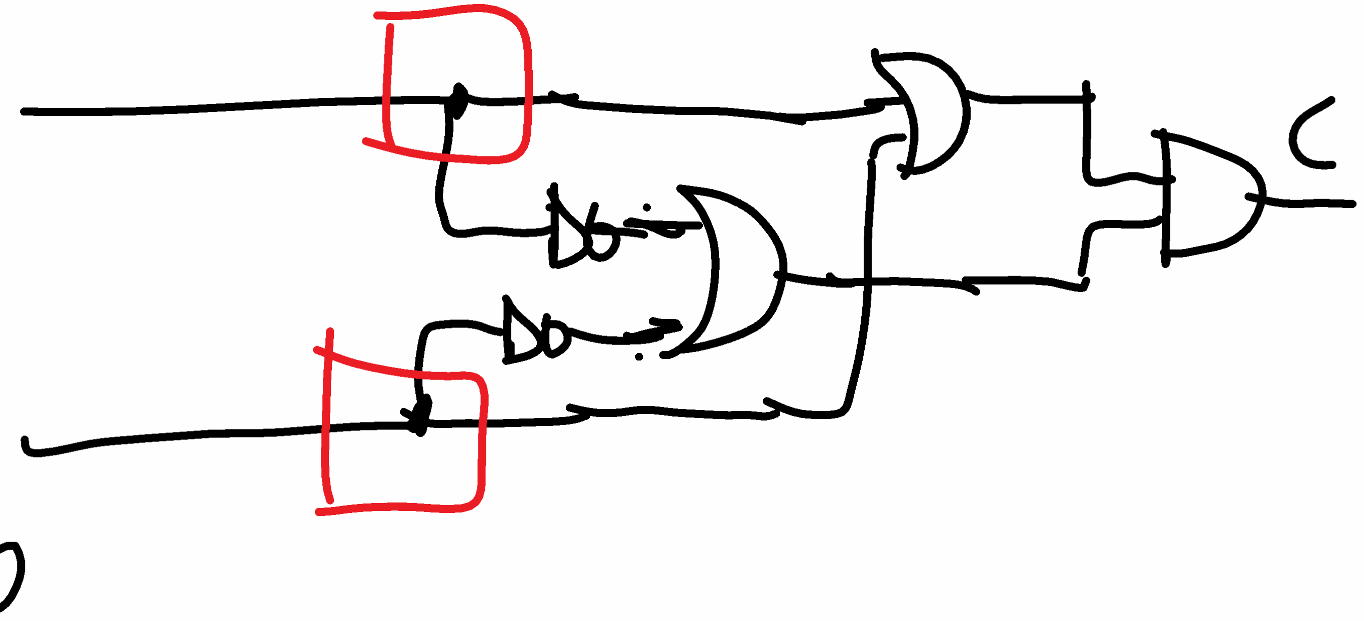
FAN OUT GATE

$$C \equiv (\neg a \wedge b) \vee (a \wedge \neg b)$$

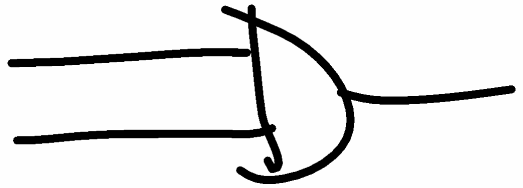
$$\equiv [\neg a \vee (a \wedge \neg b)] \wedge [b \vee (a \wedge \neg b)]$$

$$\equiv (\neg a \vee \neg b) \wedge (b \vee a)$$

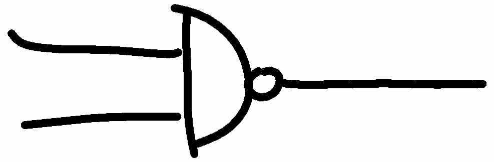
$\equiv$



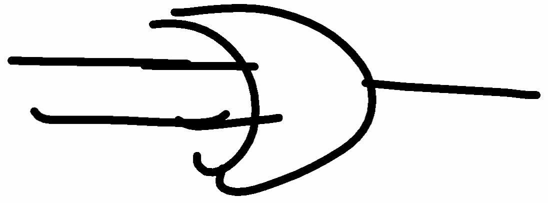
SUMMARY CLASSICAL GATES



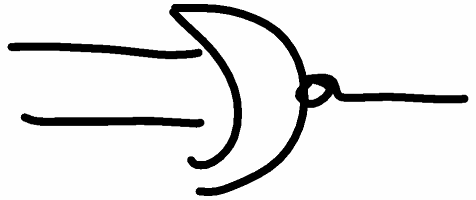
AND



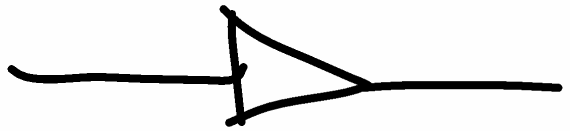
NAND



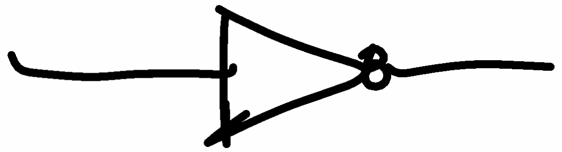
OR



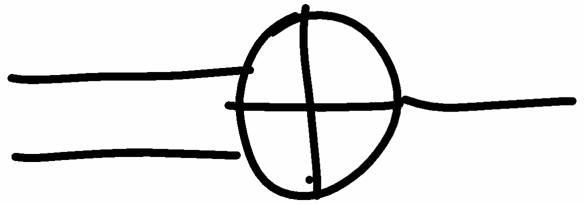
NOR



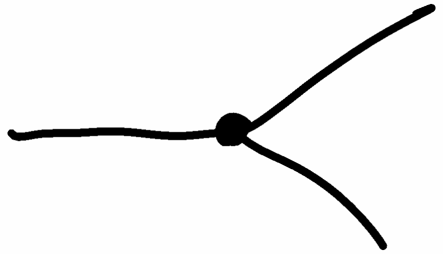
Identity



Negation



XOR

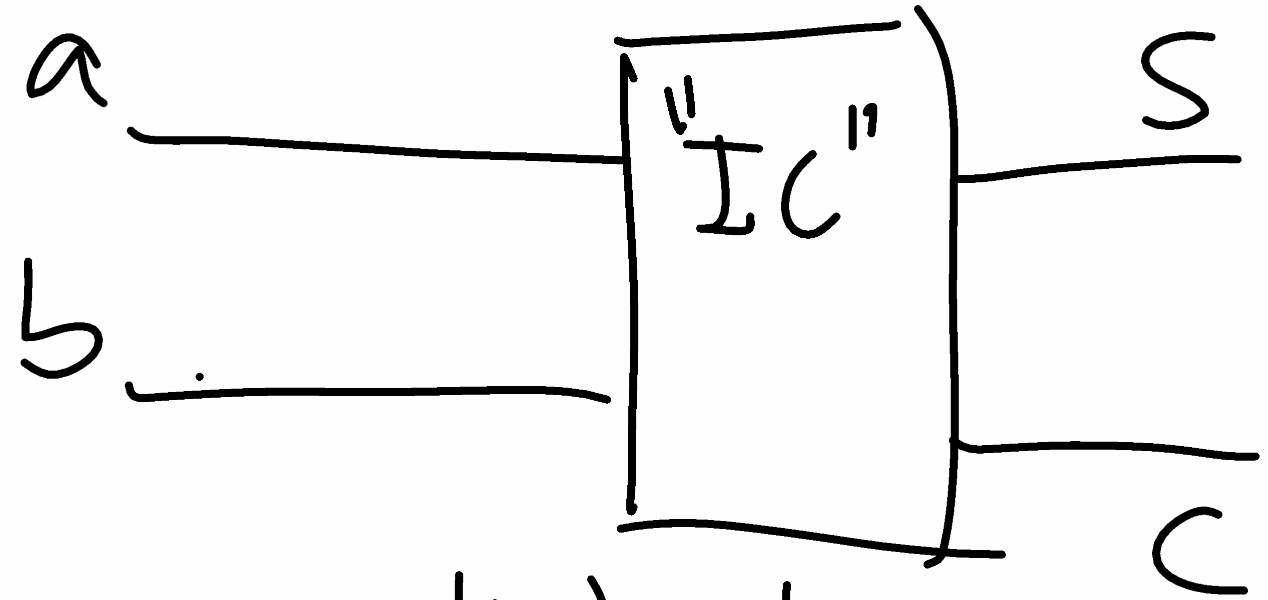


Fan-out

CIRCUITS

ADDER

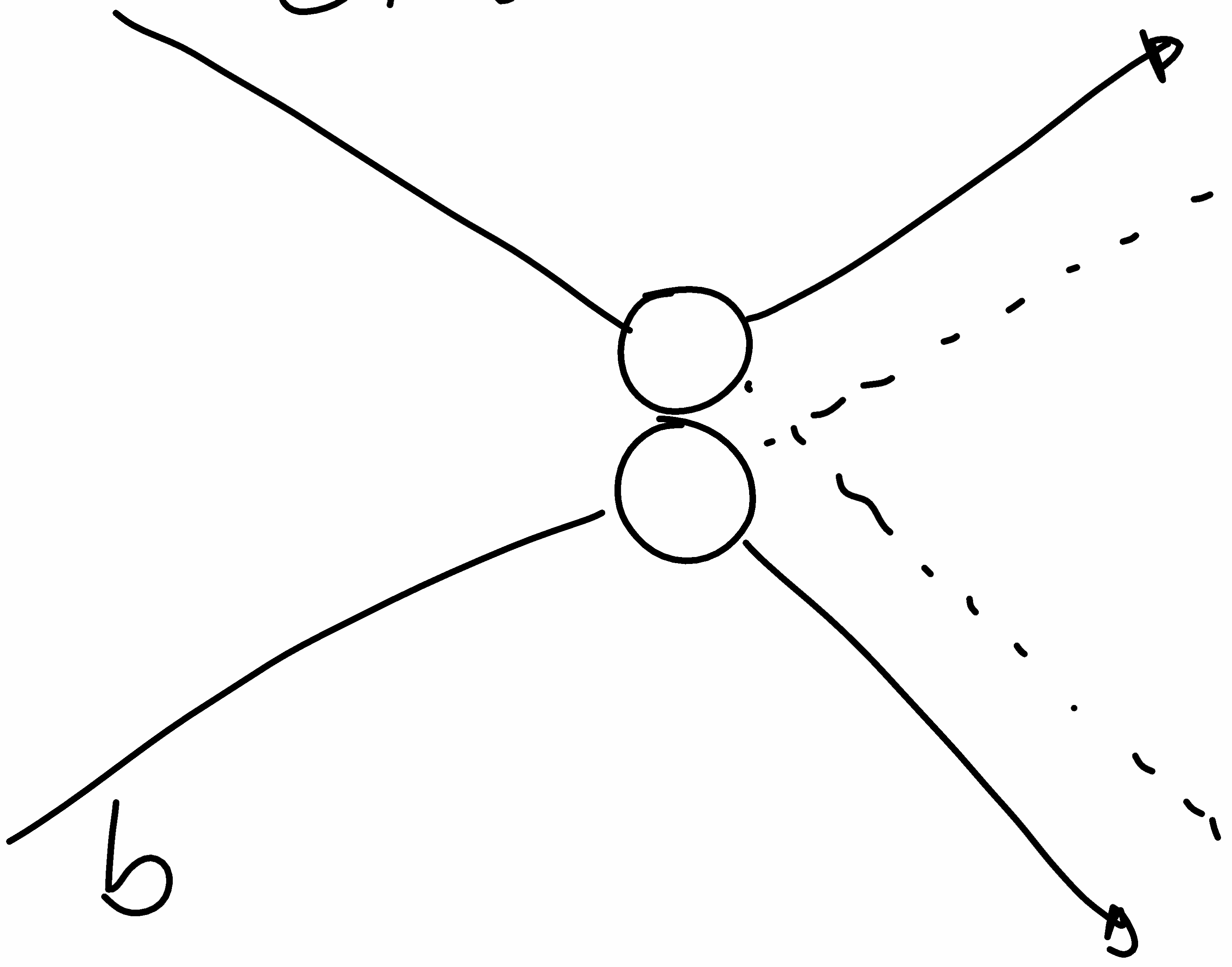
1-bit ADDER



a	b	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = a \oplus b$$
$$C = a \wedge b$$

a BILLIARD COMPUTER



$A = a \wedge b$

$B = b \wedge \neg a$

$C = \neg b \wedge a$

$D = a \wedge b$